LINEAR PHASE DETECTOR FOR HIGH-SPEED CLOCK AND DATA RECOVERY

ABSTRACT OF THE DISCLOSURE

Methods and apparatus for recovering a clock and data from a data signal. A method provides for receiving a clock signal having a first clock frequency and alternating between a first level and a second level, and receiving a data signal having a first data rate, the first data rate equal to the first clock frequency. The method also includes providing a first signal by storing the data signal when the clock signal alternates from the first level to the second level, and providing a second signal by passing the first signal when the clock signal is at the first level, and storing the first signal when the clock signal is at the second level. A third signal is provided by delaying the data signal an amount of time. An error signal is provided by combining the first signal and the third signal, and a reference signal is provided by combining the first signal and the second signal.